BYTE ALIGNMENT FOR SERIAL DATA RECEIVER

Abstract of the Disclosure

[0043]   A serial data interface for a programmable logic
device includes a receiver that deserializes a plurality
5   of channels of received serial data using a recovered
clock signal or a phase-aligned received clock signal.
Byte boundaries are initially assigned, perhaps
arbitrarily, and the deserialized signal is sent to the
programmable logic core of the programmable logic device.
10   Programmable logic in the core monitors the byte
boundaries on each channel based on the criteria,
including any user-defined parameters, programmed into the
logic. If a boundary misalignment is detected, a signal
is send from the core to bit-slipping circuitry on that
15   channel of the interface to adjust the boundary. The
signal could instruct the bit-slipping circuitry to adjust
the boundary by the number of bits needed to correct the
alignment. Alternatively, the bit-slipping circuitry
could operate iteratively, adjusting the boundary by one
20   bit, each cycle, until the signal stops indicating
misalignment.